

CLAIMS

Having thus described our invention, and what we claim as new and desire to secure by Letters Patent is:

1 1. A method for characterizing circuit activity in an IC
2 comprising: activating an IC, resolving the switching
3 activity in space and time; generating a representation
4 of the switching behavior which differentiates the time
5 that circuits or transistors switch.

1 2. A method for characterizing circuit activity in
2 integrated circuits (IC), comprising:
3 generating and applying signals to an
4 integrated circuit (IC) to cause repeated switching
5 activity in a region of interest in the IC, wherein said
6 switching activity generates emissions from said region
7 of interest;
8 recording data values identifying locations and
9 times of said emissions;
10 assigning the emissions to circuit elements or
11 devices in the region of interest;
12 processing the recorded data values to create
13 emission waveforms; and
14 analyzing the emission waveforms to
15 characterize circuit elements or devices in the region of
16 interest.

1 3. A method according to Claim 2, wherein the signals
2 are instruction sequences applied into memory elements of
3 the IC under system operations, and the signals initiate
4 execution of a sequence loop to cause repeated

5 stimulation of circuit elements or devices in the region
6 of interest.

1 4. A method according to Claim 2, wherein the signals
2 are a set of vectors or inputs applied to primary inputs
3 of the IC.

1 5. A method according to Claim 2, wherein said switching
2 activity generates optical emissions, and the recording
3 step includes the step of recording time resolved optical
4 emissions generated by the switching activity.

1 6. A method according to Claim 2, wherein the assigning
2 step includes the step of using a layout vs. schematic
3 (LVS) extraction to assign the emissions to the circuit
4 elements or devices.

1 7. A method according to Claim 2, wherein the assigning
2 step includes the step of automatically assigning the
3 emission to the circuit element using information from a
4 LVS extraction.

1 8. A method according to Claim 2, wherein the assigning
2 step includes the step of semiautomatically assigning the
3 emissions to circuit elements by having a user add or
4 subtract circuit elements to the region of interest.

1 9. A method according to Claim 2, wherein the analyzing
2 step includes the steps of:
3 analyzing the emission waveforms to identify
4 timing and/or logic behavior; and

5 comparing said timing and/or logic behavior to
6 behavior expected from electrical circuit stimulation.

1 10. A method according to Claim 2, wherein the analyzing
2 step includes the steps of:

3 analyzing the emission waveforms to identify
4 logic behavior; and

5 comparing said logic behavior to behavior
6 expected from logic stimulation.

1 11. A method according to Claim 2, wherein the analyzing
2 step includes the steps of:

3 using a known good circuit to obtain standard
4 waveforms and/or image sequences; and

5 comparing the emission waveforms to said
6 standard waveforms and/or image sequences.

1 12. A system for characterizing circuit activity in
2 integrated circuits, comprising: means for activating an
3 IC or system of ICs, means for detecting and recording
4 the switching activity of the IC(s), and a means of
5 representing the switching activities such that these may
6 be characterized.

1 13. A system according to claim 12, further comprising
2 an IC design viewer which provides a means to view the
3 measured switching activity spatially and/or temporally.

1 14. A system according to Claim 13 further comprising
2 means to identify and thereby relate the switching
3 devices/circuits between the IC design viewer
4 representations.

1 15. A system according to Claim 14 where the switching
2 data is comprised of photon emissions and the IC design
3 viewer is enabled to display emission images.

1 16. A system according to Claim 15, where the emission
2 image(s) is(are) related to the design data (physical
3 layout and/or circuit schematic and/or netlist).

1 17. A system according to Claim 15 where pixels, or
2 other such units of areal designation are assigned to
3 transistors or devices or circuits.

1 18. A system according to claim 17 where the pixels, or
2 other such unit of areal designation, are assigned
3 automatically by relating to the areal
4 transistor/device/ckt designations.

1 19. A system according to Claim 17 where the pixels or
2 other such units of areal designation are adjusted semi-
3 automatically by a user interface whereby the user may
4 indicate the pixels or regions desired for removal from,
5 or addition to, the set of pixels or regions assigned to
6 the device or transistor.

1 20. A system according to claim 19 where the graphical
2 user interface enable "point and click" selection and
3 deselection of pixels or regions.

1 21. A system according to Claim 19 where the graphical
2 user interface shows questionable pixel or region
3 designations where the user may wish to provide a choice.

1 22. A system according to Claim 15 where emission
2 waveforms are viewable from the IC viewer.

1 23. A system according to claim 16 where emission
2 waveforms are generated by a program from the areal
3 designations per transistor, device, or circuit.

1 24. A system according to Claim 23 where the emissions
2 waveforms are generated automatically when the user
3 selects the option from the IC viewer control panel.

1 25. A system according to Claim 23 where the waveforms
2 are generated automatically from the areal designations
3 and are available for view either automatically or when
4 requested, from the IC viewer.

1 26. A system according to Claim 21 where the waveform
2 viewer and emission viewer are related and are cross
3 probable.

1 27. A system according to Claim 22 where the waveforms
2 and/or images are further viewable according to the
3 design data hierarchy.

1 28. A system according to Claim 15 wherein clock
2 distribution analysis and skew characterization is
3 included.

1 29. A system according to claim 15 wherein areal regions
2 are related to a common time-base by designation of a
3 timing reference such as a reference signal contained in
4 each region.

1 30. A system according to claim 29 which electronically
2 combines regions to create a whole, or combined,
3 visualization; the combined visualization may be in the
4 form of a vide, still images, or waveforms.

1 31. A system for characterizing circuit activity in
2 integrated circuits, comprising:

3 means for generating and applying signals to an
4 integrated circuit (IC) to cause repeated switching
5 activity in a region of interest in the IC, wherein said
6 switching activity generates emissions from said region
7 of interest;

8 means for recording data values identifying
9 locations and times of said emissions;

10 means for processing the recorded data values
11 to create emission waveforms; and

12 means for analyzing the emission waveforms to
13 characterize circuit elements or devices in the region of
14 interest.

1 32. A system according to Claim 31, further comprising a
2 processor board for mounting the IC.

1 33. A system according to Claim 31, wherein the means
2 for receiving the emissions includes an optical emission
3 measurement system.

1 34. A system according to Claim 31, wherein the means
2 for generating and applying the signals includes a system
3 test computer.

1 35. A system according to Claim 31, wherein the
2 analyzing means includes a computer.

1 36. A system according to Claim 31, wherein the means
2 for generating and applying the signals includes an
3 integrated circuit tester.

1 37. A system according to Claim 31, wherein the
2 analyzing means includes an input for receiving a normal
3 time-range input by a user.

1 38. A system according to claim 31, wherein the
2 analyzing means includes a software utility for supplying
3 normal time ranges.

1 39. A system according to Claim 31, wherein the
2 analyzing means includes:
3 means for recording an expected behavior,
4 including means for extracting from the waveforms a
5 transition of a circuit element or device from a first
6 state to a second state, and for recording an expected
7 time for said transition from the application of a
8 predetermined one of the signals.

1 40. A system according to Claim 31, wherein the region
2 of interest includes input and output nets, each of the
3 input and output nets having a logic state, and wherein
4 the analyzing means includes means for recording a
5 transition expected from the logic states at the input
6 and output nets at a given time determined by a gate
7 level simulation of the IC.

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41. A system according to Claim 31, wherein the analyzing means includes means for flagging the occurrence of predefined peaks or the absence of predefined peaks, and said flagging means includes a software utility that compares the emission waveform to expected behavior data stored in a computer file.

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42. A system according to Claim 31, wherein:
the analyzing means includes means for flagging emissions that occur at wrong times; and
said flagging means includes a software utility that compares the times of switching activity to expected times stored in a computer file, and that checks to determine if the switching activity is in a previously defined acceptable range.

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43. A method for analyzing an integrated circuit, comprising:
detecting a fault in the circuit;
applying known stimulus to the circuit to reproduce the fault and to localize the fault to a component of the circuit;

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the circuit component;
collecting time resolved light emissions from the circuit component;
analyzing the collected time resolved light emissions to extract switching and timing data about the circuit components; and
comparing the extracted switching and timing data to expected switching and timing behavior data to characterize the fault.

1 44. A method according to Claim 43, wherein the
2 comparing step includes the step of comparing extracted
3 data to expected behavior data to identify (i) missing
4 switching events, and (ii) switching events that should
5 not have occurred..

1 45. A method according to Claim 43, wherein the
2 comparing step includes the step of comparing extracted
3 data to expected behavior data to detect early switching
4 events and late switching events.